

OPN Certified Specialist 1Z0-489

SPARC M6-32 and SPARC M5-32 Servers Installation Essentials

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D. Connect Category 6 (or better) cables and network devices that support 1000BASE-T networks to separate terminal devices

Answer: D

Explanation:

Reference:

https://docs.oracle.com/cd/E24355_01/html/E41214/z4000b7d1393076.html

Question: 4

When booting up a pre-installed domain, you are asked for some configuration information. Where should you look for that information?

- A. System Administration Guide
- B. Installation and Configuration Plan
- C. Installation Guide
- D. Server Product Notes

Answer: C

Explanation:

Reference:

<https://www.debian.org/releases/stable/armel/install.txt.en>

Question: 5

During a site visit to a customer who has three SPARC M5-32 platforms, which two actions would you take to confirm each platform serial number?

- A. Visually check for the chassis serial number label at the front lower left – hand side.
- B. Using the SP on each platform to access the ILOM, run show /system serial_ number.
- C. Visually check for the chassis serial number label at the front upper right-hand side.
- D. Using the SP on each platform to access the ILOM, run show /systemsystem_ identification.
- E. Visually check for the chassis serial number label at the rear, towards the top, in the middle.

Answer: B,D

Explanation:

Reference:

https://docs.oracle.com/cd/E19203-01/820-1188-12/core_ilom_overview.html

Question: 6

Which three statements are correct about data paths in the SPARC M5-32 server?

- A. Within a DCU, a CPU talks to another CPU directly by using the coherency switch. The SSB is not needed.
- B. From one DCU to a different DCU, an even talks with only another even (same for odd) and hops to the odd-numbered board, if needed, on the destination DCU.
- C. From one DCU to a different DCU, all CPUs can access all PCIe slots in the destination DCU directly in one hop.
- D. A DCU can communicate data only with other DCUs via the BX ASICs on the SSB.
- E. From one DCU to a different DCU, even CPUs can access all the odd PCIe slots in the destination DCU directly in one hop.

Answer: A,C,D

Explanation:

Reference:

http://docs.oracle.com/cd/B10501_01/server.920/a96533/statspac.htm

Question: 7

Which statement is correct?

- A. The SPARC M5-32 processor has 16 cores, 48MB L3\$; T5 processor has 16 cores, 8MB L3\$
- B. The SPARC M5-32 processor has 6 cores, 48MB L3\$; T5 processor has 16 cores, 8MB L3\$
- C. The SPARC M5-32 processor has 16 cores, 24MB L3\$; T5 processor has 16 cores, 8MB L3\$
- D. The SPARC M5-32 processor has 6 cores, 24MB L3\$; T5 processor has 16 cores, 48MB L3\$

Answer: B

Explanation:

Reference:

http://docs.oracle.com/cd/E24355_01/html/E41214/z40001331392991.html

Question: 8

You power -on PDomain0 and notice that it does not go through POST, Examine the following output:

```
-> show /HOST0/diag
Targets:
Properties:
error_reset_level = max
error_reset_verbosity = normal
hw_change_level = max
hw_change_verbosity = normal
level = max
mode = off
power_on_level = max
power_on_verbosity = normal
trigger = hw-change error-reset
verbosity = normal
<SNIP>
```

In order for this to go through post, which property needs to be changed?

- A. level
- B. mode
- C. power_on_level
- D. error_reset_level

Answer: C

Question: 9

Which three statements are true about the newest clock board redesign/ operation in a SPARC M5-32/M6-32 server?

- A. There are two clock boards in a redundant configuration, so the failure of the primary clock board does not cause a reboot of the server.
- B. There are two clock boards. Each has two clock sources, so if a clock source fails, the alternate clock source on the same board takes over.
- C. While the system is running on an active clock board, a faulty clock board can be replaced dynamically.
- D. There are two clock boards in a redundant configuration, and there is a dynamic failover of the primary clock board to the standby clock board.

Answer: A,B,D

Question: 10

Which three statements are correct about installing DIMMS?

- A. Be sure that you are properly grounded before inserting the DIMM(s) in the socket(s).
- B. If a DIMM slot LED is lit, press the Fault Remind button to turn off the LED.
- C. When replacing a faulty CMU, you do not need to keep DIMMs in the same locations on thereplacement CMU, because the server has an intelligent load-balance feature.
- D. When you press the DIMM Fault Remind button, the slot for a faulty DIMM is lit.
- E. If a DIMM slot LED is lit, the fault is cleared only by the reset command In JLOM.

Answer: B,C,D

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